TAA2009

STEREO 9W (8Ω) CLASS-T™ DIGITAL AUDIO AMPLIFIER USING DIGITAL POWER PROCESSING™ TECHNOLOGY

TECHNICAL INFORMATION **Revision 1.02 – May 2006**

GENERAL DESCRIPTION

The TAA2009 is a 9W/ch continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. The TAA2009, in a QFN package, along with extremely high efficiency, allows for a very compact amplifier design. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

- LCD TV's
- LCD Monitors
- Plasma TV's
- Computer/PC Multimedia
- Battery Powered Systems

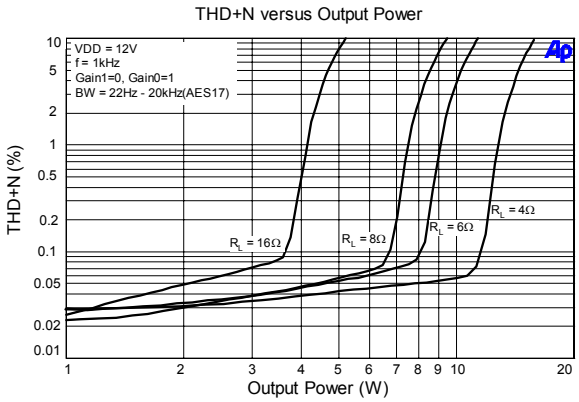
BENEFITS

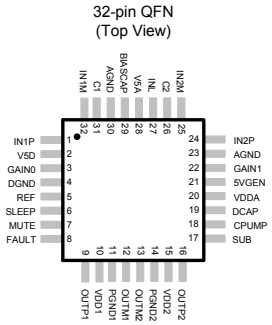
- Fully integrated solution with FETs
- Compact packaging and board design
- Reduced system cost with no heat sink
- Differential inputs minimize common-mode noise
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and Internet audio
- Capable of driving a wide range of load impedances
- Sophisticated pop reduction circuit

FEATURES

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.05% THD+N @ 5W, 8Ω
  - 0.16% IHF-IM @ 1W, 8Ω
  - 6.4W @ 8Ω, 0.1% THD+N
  - 3.5W @ 16Ω, 0.1% THD+N
- High Power
  - 10.6W @ 6Ω, 10% THD+N
  - 9W @ 8Ω, 10% THD+N
  - 5W @ 16Ω, 10% THD+N
- Extremely High Efficiency
  - 90% @ 5W, 16Ω
  - 86% @ 9W, 8Ω
- Dynamic Range = 96 dB
- Mute and Sleep modes
- Improved turn-on & turn-off pop suppression
- Over-current protection with automatic restart circuit
- Over-temperature protection
- Space saving 32-pin 8mm x 8mm x 1mm QFN package with exposed pad
- Filterless Operation Option

TYPICAL PERFORMANCE





ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER	Value	UNITS
V_{DD}	Supply Voltage (note 1)	14	V
MUTE, SLEEP, GAIN1, GAIN0, INL	MUTE Input Voltage	-0.3 to V5 + 0.3	V
T_{STORE}	Storage Temperature Range	-40 to 150	°C
T_A	Operating Free-air Temperature Range	-40 to +85	°C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 2)	1500	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Please note that this is not a valid "operating condition". The maximum voltage on the VDD pins during operation is 13.2V. Refer to the Maximum Supply Voltage section on page 13.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.

OPERATING CONDITIONS (Note 3)

-40°C to +85°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage (note 1)	8.5	12	13.2	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP, GAIN1, GAIN0, INL)	4.2			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP, GAIN1, GAIN0, INL)			1.0	V

Note 3: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNITS
θ_{JA}	Junction-to-ambient Thermal Resistance (note 4)	21	°C/W

Note 4: The θ_{JA} value is based on the exposed pad being soldered down to the printed circuit board. The exposed pad must be soldered to an exposed copper area on the printed circuit board for proper thermal and electrical performance. The exposed pad is at substrate ground.

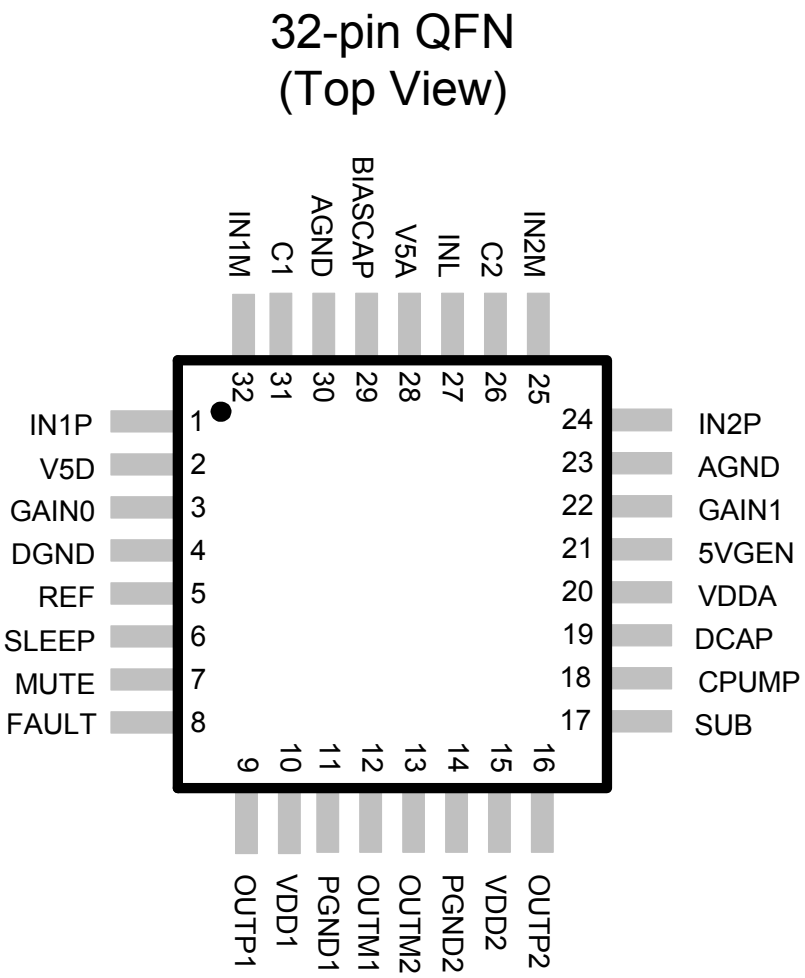
ELECTRICAL CHARACTERISTICS (Note 5)

See Application/Test Circuit with single ended inputs and filtered outputs. Unless otherwise specified, V_{DD} = 12V, f = 1kHz, Gain1=0, Gain0=1 Measurement Bandwidth = 20kHz, R_L = 8Ω, T_A = 25 °C, package exposed pad soldered to the printed circuit board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous Average/Channel)	THD+N = 0.1% R_L = 6Ω R_L = 8Ω R_L = 16Ω THD+N = 10% R_L = 6Ω R_L = 8Ω R_L = 16Ω		7.8 6.4 3.5 10.6 9 5		W W W W W W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		28		mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		7		mA
I_q	Quiescent Current	V_{IN} = 0 V		60		mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 5W/Channel		0.05		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), Po = 1W		0.16		%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 9W, R_L = 8Ω		96		dB
CS	Channel Separation	f = 1 kHz 20 Hz ≤ f ≤ 20 kHz		96 70		dB dB
PSRR	Power Supply Rejection Ratio	VDD = 9V to 13.2V		85		dB
η	Power Efficiency	P_{OUT} = 9W/Channel, R_L = 8Ω		86		%
$V_{OFFSET1}$	Dynamic Output Offset Voltage (note 6)	MUTE transition from high to low	-10		10	mV
$V_{OFFSET2}$	Static Output Offset Voltage	MUTE = low		50		mV
V_{OH}	High-level output voltage (FAULT)	-40°C to +85°C, I_{OH} = 250uA	4.5			V
V_{OL}	Low-level output voltage (FAULT)	-40°C to +85°C, I_{OL}= 250uA			0.5	V
e_{OUT}	Output Noise Voltage	A-Weighted, input AC grounded		160		μV

Note 5: Minimum and maximum limits are guaranteed but may not be 100% tested.
Note 6: Refer to the Dynamic DC Offset Calibration section on page 14 for a detailed description of Dynamic Offset Voltage.

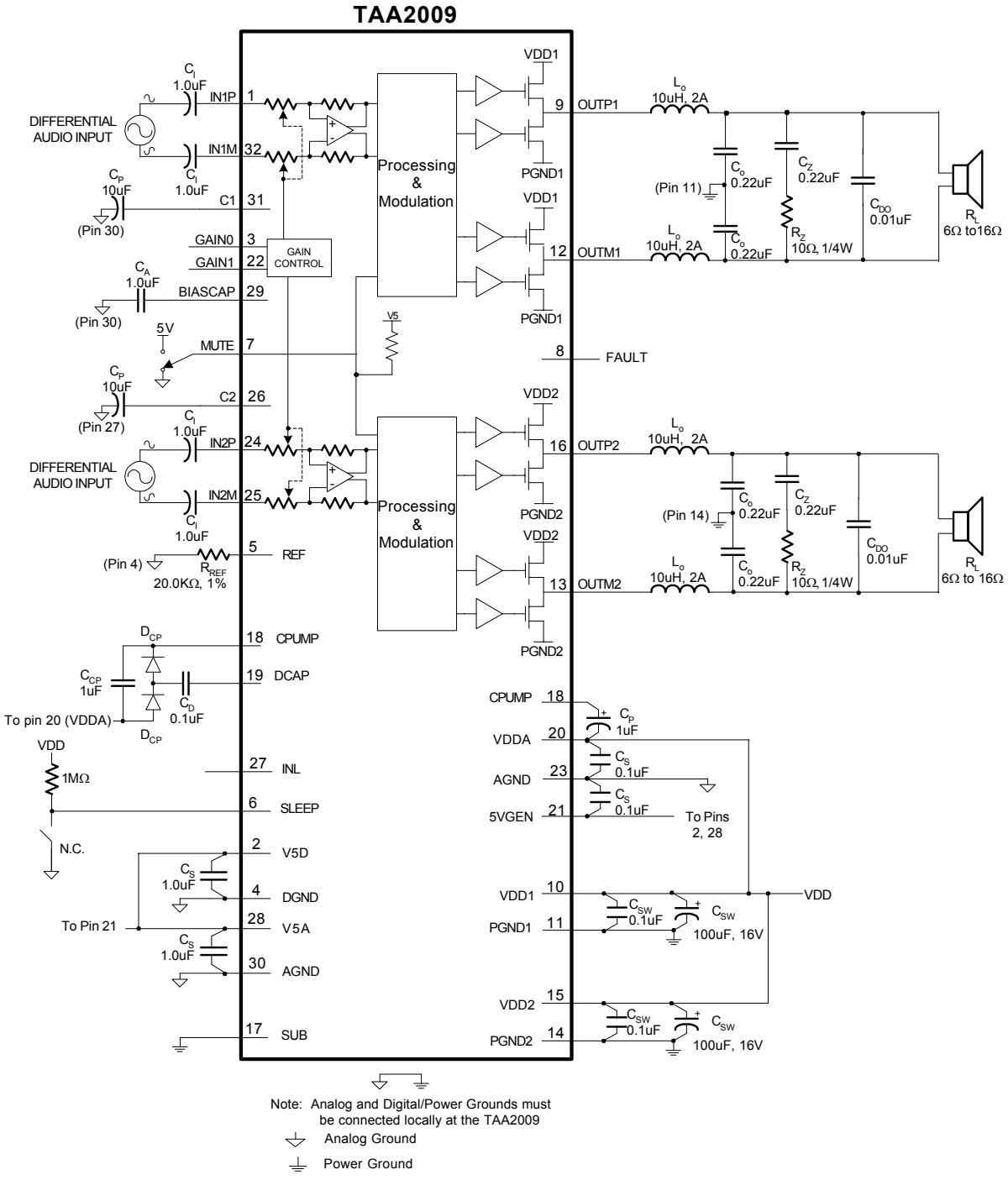
TAA2009 PINOUT



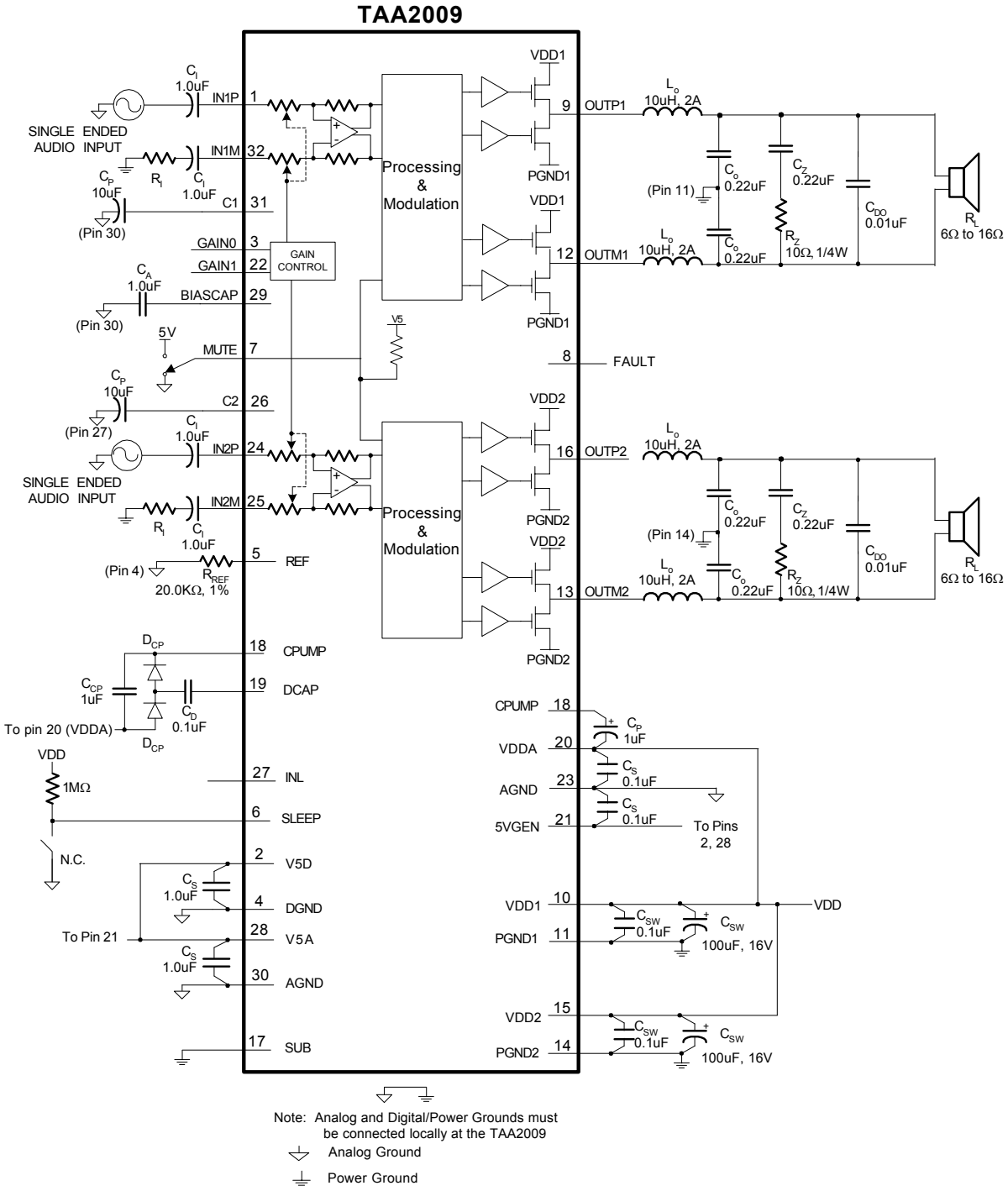
PIN DESCRIPTION

Pin	Function	Description
1, 24	IN1P, IN2P	Positive audio input for channel 1 and channel 2
2, 28	V5D, V5A	Digital 5VDC, Analog 5VDC
3, 22	GAIN0, GAIN1	Gain select bits. GAIN0 is least significant bit. See Applications Information for programmable gain values. Both GAIN 0 and GAIN1 have internal 50KΩ pull-down resistors.
4	DGND	Digital Ground. Connect to AGND locally (near the TAA2009).
5	REF	Internal reference voltage; approximately 1.0 VDC.
6	SLEEP	When set to logic high, device goes into low power mode. If not used, this pin should be grounded
7	MUTE	When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. This pin should be tied to GND if not used.
8	FAULT	A logic high output indicates an under-voltage condition, thermal overload, and an output is shorted to ground, or another output.
9, 12 16, 13	OUTP1 & OUTM1 OUTP2 & OUTM2	Bridged output pairs
10, 15	VDD1, VDD2	Supply pins for high current H-bridges, nominally 12VDC.
11, 14	PGND1, PGND2	Power Grounds (high current)
17	SUB	Substrate connection. Connect to PGND.
18	CPUMP	Charge pump input (nominally 10V above VDDA)
19	DCAP	Charge pump switching output pin. DCAP is a free running 350kHz square wave between VDDA and DGND (12Vpp nominal).
20	VDDA	Power supply for analog VDD circuitry. Connect to same supply as VDD1 and VDD2.
21	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 2 and 28).
23, 30	AGND, AGND	Analog Ground. Connect all pins together directly at the TAA2009.
25, 32	IN2M, IN1M	Negative audio input for channel 2 and channel 1.
26, 31	C2, C1	Pop minimization capacitor. Use 10uF.
27	INL	Modulation selection pin. Connecting the INL pin to a logic high level enables the inductor-less mode. This mode allows the TAA2009 to be operated without an output filter as the switching outputs are in phase with zero input. If INL is tied to a logic low or left floating (pulled down via internal 50KΩ resistor to ground), the INL mode will be disabled. This results in a differential output switching pattern typical of previous Tripath generation parts such as TA2024 and TAA2008. The state of the INL pin should only be changed with MUTE at a logic high state.
29	BIASCAP	Input stage bias voltage (approximately 2.4VDC).

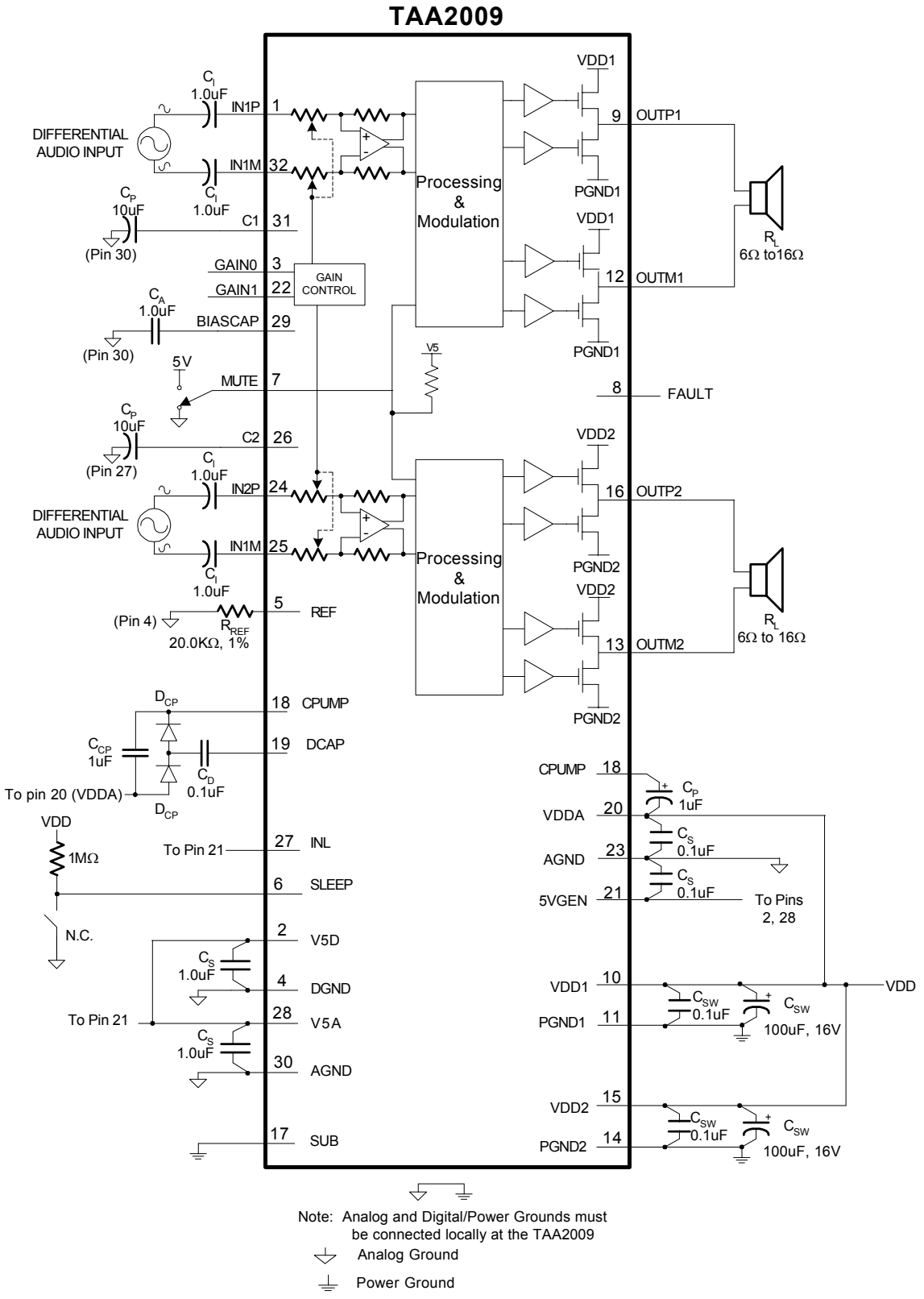
APPLICATION / TEST CIRCUIT WITH DIFFERENTIAL INPUTS AND FILTERED OUTPUTS



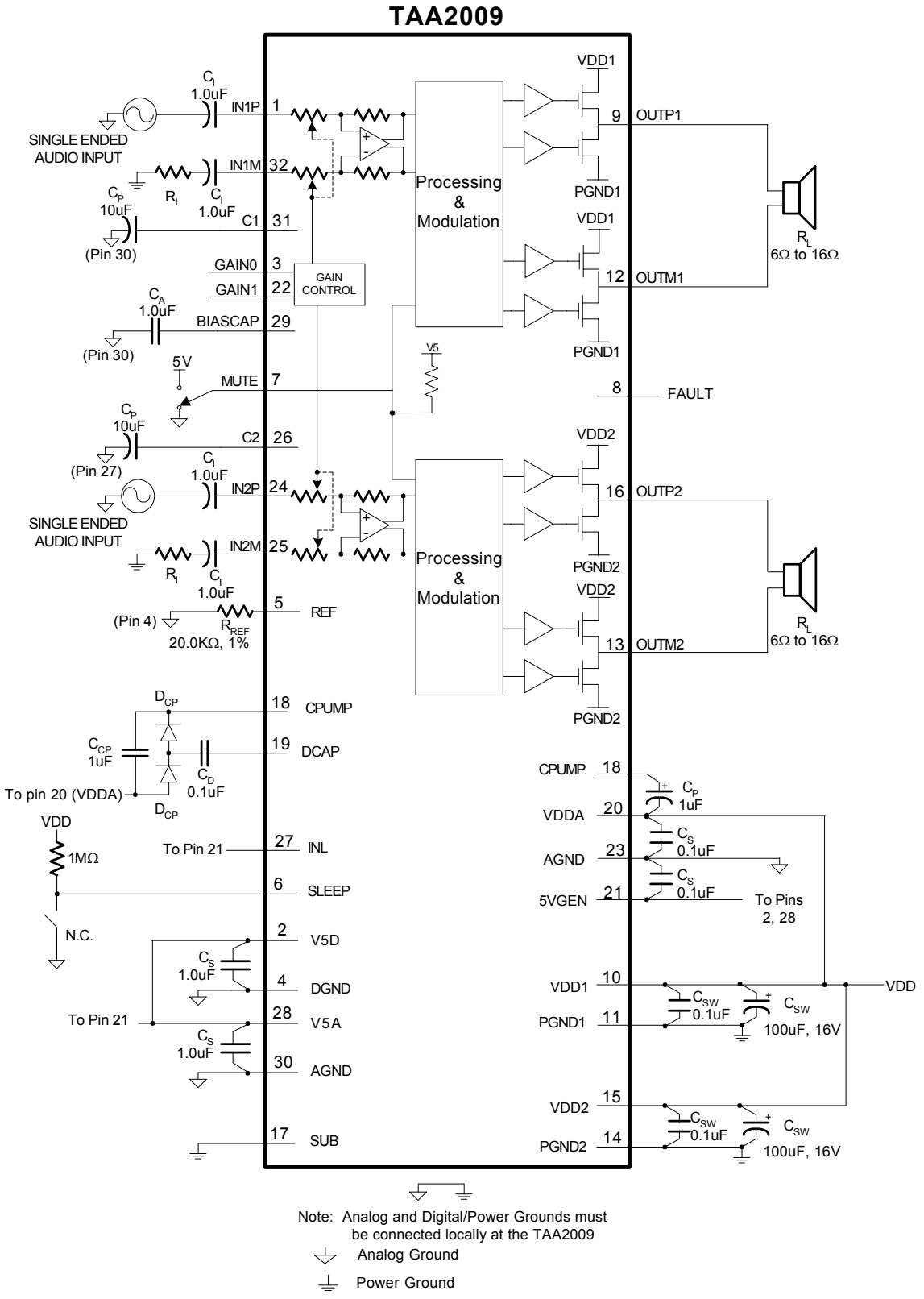
APPLICATION / TEST CIRCUIT WITH SINGLE ENDED INPUTS AND FILTERED OUTPUTS



APPLICATION / TEST CIRCUIT WITH DIFFERENTIAL INPUTS AND FILTERLESS OUTPUTS



APPLICATION / TEST CIRCUIT WITH SINGLE ENDED INPUTS AND FILTERLESS OUTPUTS

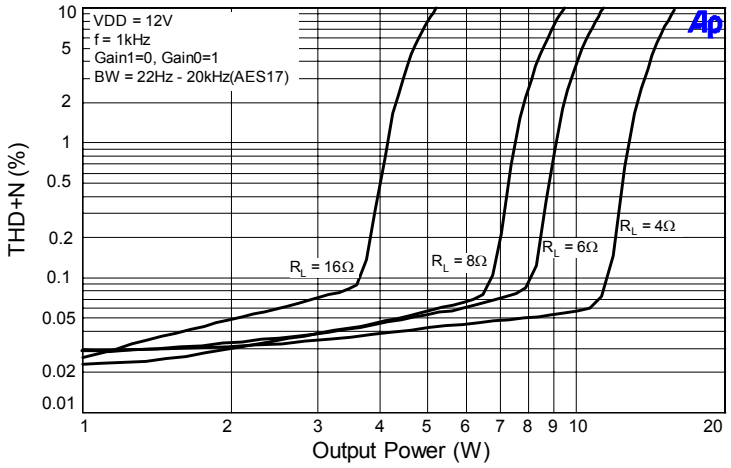


External Components Description (REFER TO THE APPLICATION/TEST CIRCUIT)

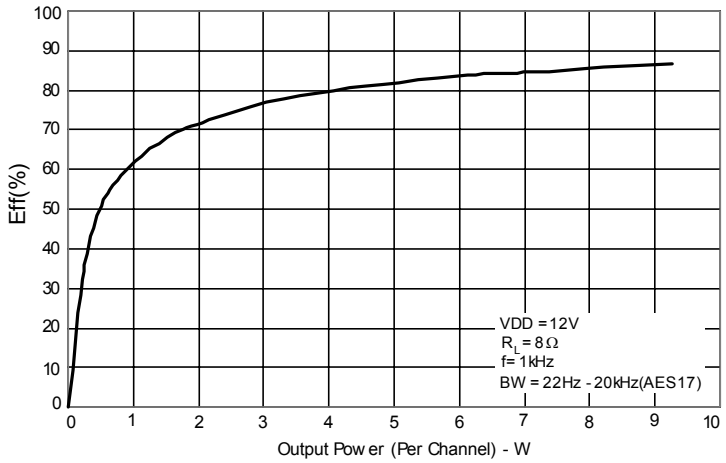
Components	Description
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$
R_I	Input resistor. Used only in applications where the audio source has a single ended output. The resistor value should match the audio source's output impedance.
C_P	Capacitor used to eliminate turn-on and turn-off pops. One capacitor is used for each channel. Please use 10uF for this capacitor. This resistor should be grounded at the same channels C_{SW} ground connection.
R_{REF}	Bias resistor. Locate close to pin 25 (REF) and ground at pin 24 (AGND1).
C_A	BIASCAP decoupling capacitor. Locate close to pin 3 (BASCAP) and ground at pin 4 (AGND3).
C_D	Charge pump input capacitor. This capacitor should be connected directly between pins 19 (DCAP) and the external diodes (D_{CP}) and located physically close to the TAA2009.
D_{CP}	External diodes used to create charge pump power supply. Please refer to the Application / Test Circuit for proper connection
C_{CP}	Charge pump output capacitor that enables efficient high side gate drive for the internal H-bridges. To maximize performance, this capacitor should be connected directly between pin 18 (CPUMP) and pin 17 (VDDA). Please observe the polarity shown in the Application / Test Circuit.
C_S	Supply decoupling for the low current power supply pins. For optimum performance, these components should be located close to the pin and returned to their respective ground as shown in the Application/Test Circuit.
C_{SW}	Supply decoupling for the high current, high frequency H-Bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. Both the high frequency bypassing (0.1uF) and bulk capacitor (100uF/220uF) should have good high frequency performance including low ESR and low ESL. Recommended capacitor families include Nichicon HE series and Panasonic FM series for thru-hole types. Qualified SMT electrolytics include Nichicon UD series and Panasonic FK series.
C_Z	Zobel Capacitor.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with frequency.
L_O	Output inductor, which in conjunction with C_O and C_{DO}, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_{TOT}})$ and a quality factor of $Q = R_L C_{TOT}/2\sqrt{L_O C_{TOT}}$ where $C_{TOT} = C_O \parallel 2 * C_{DO}$.
C_O	Output capacitor.
C_{DO}	Differential Output Capacitor. Differential noise decoupling for reduction of conducted emissions. Must be located near chassis exit point for maximum effectiveness.

TYPICAL PERFORMANCE WITH SINGLE ENDED INPUTS AND FILTERED OUTPUTS

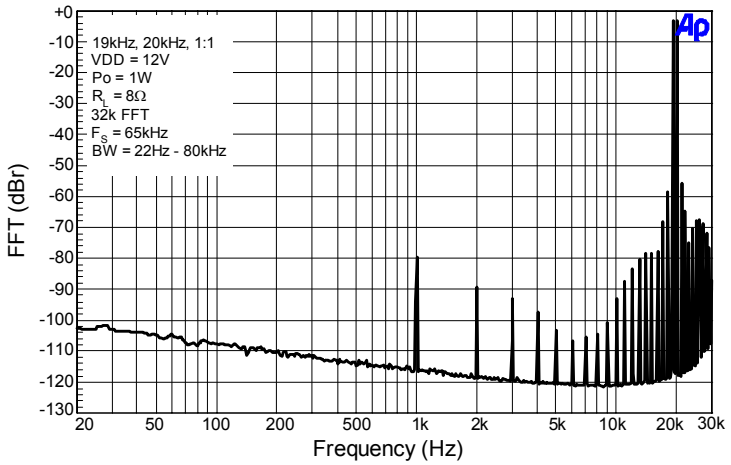
THD+N versus Output Power



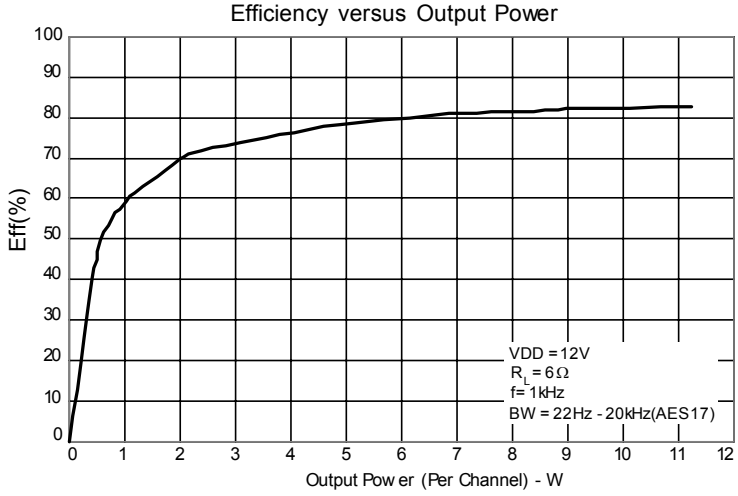
Efficiency versus Output Power



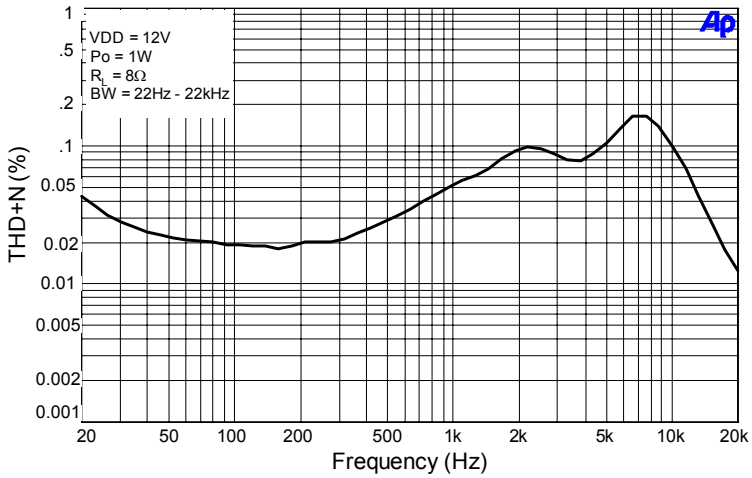
Intermodulation Distortion



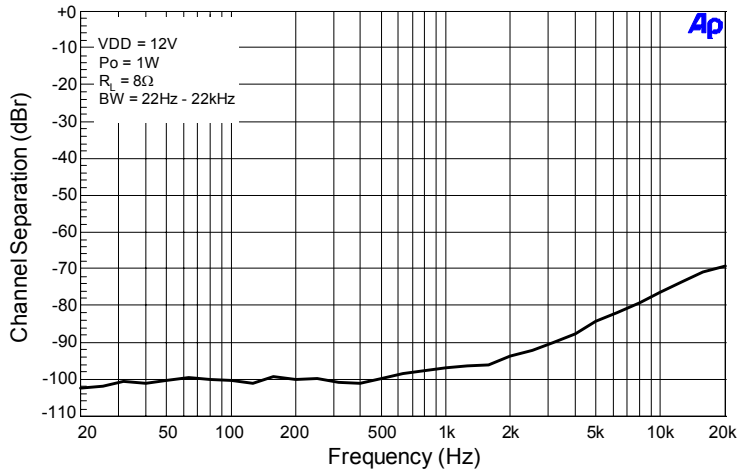
Efficiency versus Output Power



THD+N versus Frequency

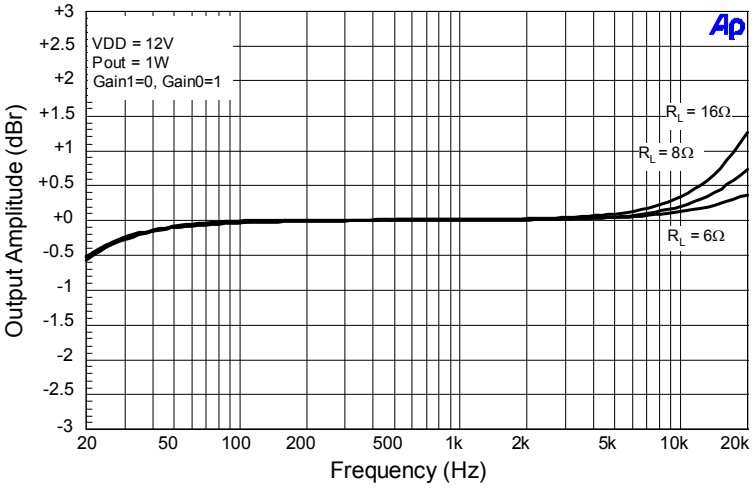


Channel Separation versus Frequency

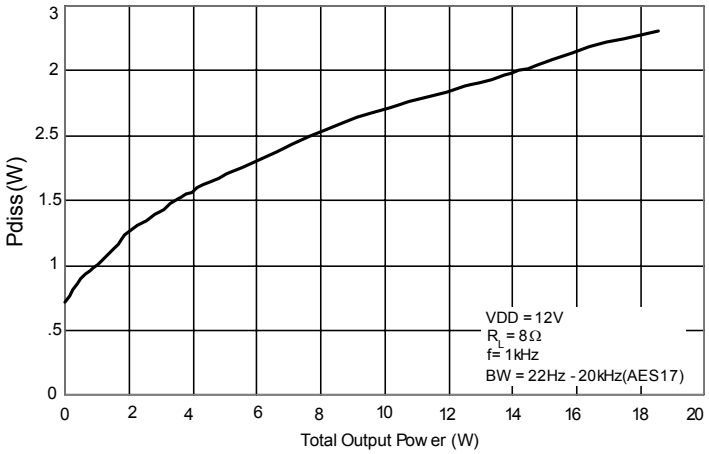


TYPICAL PERFORMANCE WITH SINGLE ENDED INPUTS AND FILTERED OUTPUTS

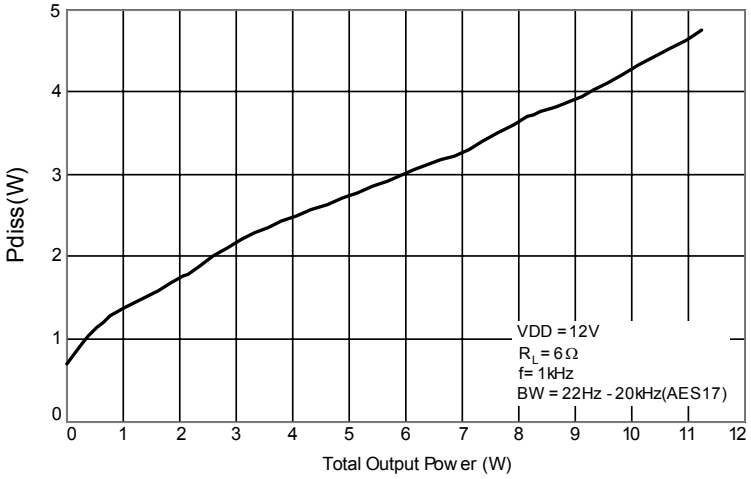
Frequency Response



Power Dissipation versus Total output Power



Power Dissipation versus Total output Power



APPLICATION INFORMATION

Layout Recommendations

The TAA2009 is a power (high current) amplifier that operates at relatively high switching frequencies. The outputs of the amplifier switch between the supply voltage and ground, at high speeds, while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TAA2009 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes. Please contact Tripath Technology for further information regarding reference design material regarding the TAA2009.

Maximum Supply Voltage

The absolute maximum allowable voltage on the VDD supply pins (pins 10, 15, and 20) is 14V. Device damage can occur above this voltage. Please note that this is not a valid "operating condition". The maximum voltage on the VDD pins during operation is 13.2V.

During normal operation, the output pins (pins 9, 12, 13, and 16) may experience overshoot voltages due to inductive kickback that are above 14V. These pins can tolerate overshoot of up to 18V. However, care should be taken to properly decouple the VDD pins. Overshoot on the output pins can travel through the TAA2009 output devices and appear on the VDD pins. Without proper power supply decoupling, this can cause ripple voltages on the VDD pins that might exceed their absolute maximum voltage. However, this will only happen in extreme cases and can be prevented by placing the high frequency decoupling capacitors close to the VDD pins.

TAA2009 Input Stage

The input stage of the TAA2009 is configured as a differential receiver to maximize common mode rejection in typical audio circuits. To maximize this benefit, the INxP and INxM should be driven with out of phase signals from sources that have the same output impedance. Also, the signal from the sources should be routed in a parallel fashion from the source.

In some instances, there will be a necessity to drive the TAA2009 with a single-ended input signal. In this case, the unused input should be AC coupled to Power Ground using the same value of C_I implemented for the driven channel. Either input, INxP or INxM, can be used for the signal input. To minimize the effects of ground noise in the system, C_I should be terminated at the C_{SW} ground connection point through a resistor. Please refer to Figure 1. The value of the resistor should match the output impedance of the audio source. Please refer to the Applications Schematic for component locations and descriptions.

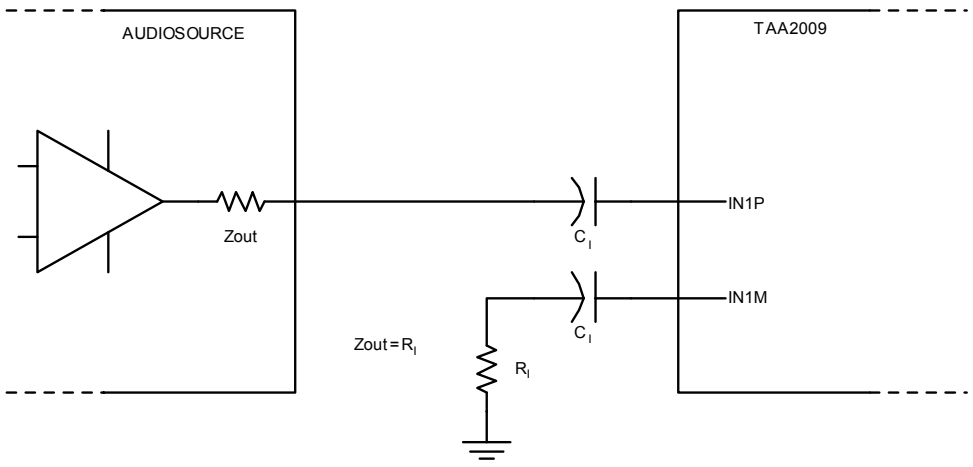


Figure 1

Dynamic DC offset Calibration

One of the major causes of turn-on and turn-off pop is DC offset. Typically, when a system turns on (begins switching), the potential across the speaker changes abruptly from 0V to whatever the DC offset voltage of the system is. Similarly, when the system turns off, the potential changes abruptly from the DC offset voltage to 0V. This abrupt change is heard as a pop.

The TAA2009 employs a patent pending method for reducing pop. At the start of switching, a calibration circuit minimizes the potential across the speaker to the “dynamic DC offset” voltage. Then, the potential is ramped up (or down) to the “static DC offset” voltage where it remains during normal operation. (See Figure 2 and Figure 3) This ramp is slow enough to keep the speaker movement in the subsonic range. During turn-off, this procedure is reversed. The static DC offset voltage is ramped down to the static DC offset level before switching stops.

Dynamic offset cancellation requires equal impedances on the positive and negative inputs. If a single ended audio source with a 600Ω output impedance is connected to IN1P (through a DC blocking capacitor), then IN1M must be terminated to ground with a 600Ω resistor (also through a DC blocking capacitor). Please refer to figure 1.

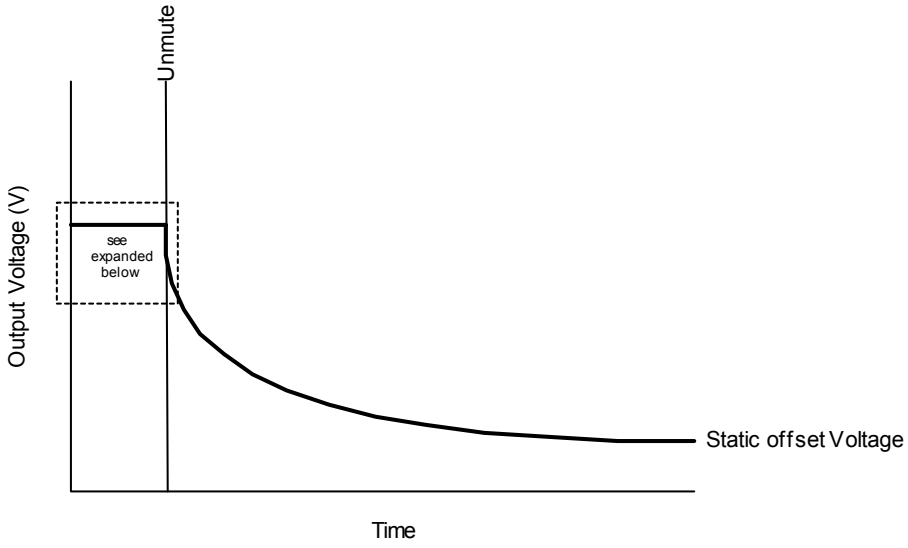


Figure 2

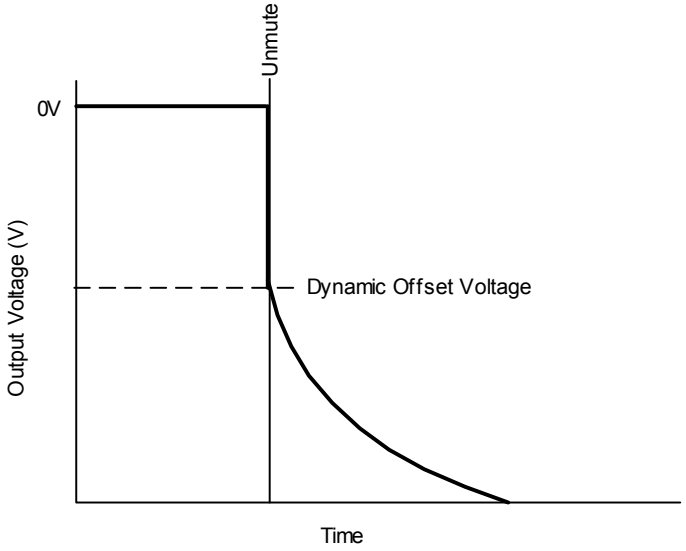


Figure 3

TAA2009 Amplifier Gain

The closed loop gain of the TAA2009 is externally configurable via two input pins, GAIN0 and GAIN1. The table below shows the three different gain values available based on the pin voltages at GAIN0 and GAIN1. Internally, different input resistor values are used to implement the three gain settings. Thus, the input impedance will change based on gain setting. The gain tracking is very tightly matched from device to device, but the absolute input impedance will vary +/-25% due to process variations. This variation must be considered when choosing the proper value of Ci (see discussion below).

TAA2009 AMPLIFIER GAIN SETTING

GAIN1	GAINO	GAIN (V/V)	GAIN (dB)	INPUT IMPEDANCE (kΩ)
0	1	12	21.6	33.95
1	0	20	26	20.4
1	1	30	29.5	13.6

The low frequency roll-off characteristic is dictated by the choice of C_I and R_I. As noted previously, the input impedance varies depending on gain setting. Based on a +/-25% variation of input resistance, the minimum input resistance is 10.2kΩ (for 30V/V gain setting) and the maximum input resistance is 84.9kΩ (for the 6V/V gain setting)

The –3dB frequency is:

$$f_{-3dB} = \frac{1}{2\Pi C_I R_I}$$

On the EB-TAA2009, a value of 1.0μF is used for C_I which creates a nearly flat response down to 20Hz even for the 30V/V gain setting. In many cases, a lower value of C_I can be used due to a lower gain setting, or because the speakers used in LCD TV's or similar applications do not have the ability to reproduce low frequency signals.

Mute Pin

The mute pin must be driven to a logic low or logic high state for proper operation. To enable the amplifier, connect the mute pin to a logic low. To enable the mute function, connect the mute pin to a logic high signal. Please note that the mute pin is a 5V CMOS input pin and the mute signal should be de-bounced to eliminate a possibility of falsely muting.

When in mute, the internal processor bias voltages are still active in the TAA2009. This minimizes any turn on pop caused by charging the input coupling capacitor. It is recommended that the mute pin is held high during power up or power down to eliminate audible transients.

If turn-on and/or turn-off noise is still present with a TAA2009 amplifier, the cause may be other circuitry external to the TAA2009 such as an audio processor or preamp. Multiple audio processors used in LCD TV's create audible pops as their power supply collapses. If the TAA2009 is still active (mute pin is low), then these audible pops will be amplified and output to the speakers. To eliminate this problem, simply activate the mute before the power supply collapses.

Sleep Pin

The SLEEP pin is a 5V logic input that when pulled high puts the part into a low quiescent current mode. To disable SLEEP mode, the sleep pin should be grounded.

INL Pin

The INL pin selects the modulation scheme mode. Connecting the INL pin to a logic high level enables the inductor-less mode. This mode allows the TAA2009 to be operated without an output filter as the switching outputs are in phase with zero input. If INL is tied to a logic low or left floating (pulled down via the internal 50KΩ resistor to ground), the INL mode will be disabled. This results in a differential output switching pattern typical of previous Tripath generation parts such as TA2024 and TAA2008.

The state of the INL pin should only be changed with MUTE at a logic high state.

Protection Circuits

The TAA2009 is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-STATED, and will float to 1/2 of V_{DD}. The amplifier will automatically attempt to recover from a fault condition every 1 second and will enter fault again, if the cause for the original fault is still present (such as a speaker output still being shorted to ground).

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

Over-current Protection

An over-current fault occurs if more than approximately 4 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground.

Fault Pin

The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. All faults automatically reset upon removal of the condition.

Power Dissipation Derating

The TAA2009, as a result of high efficiency and good package thermal characteristics, can operate at elevated ambient temperatures without having to derate the output power, assuming 8 ohm output loads or higher. This in stark contrast to many other “competitive” solutions from other semiconductor vendors, many of which can only provide full power at ambient temperatures of 25°C, or slightly higher, without exceeding a junction temperature of 150°C. Lower die temperatures result in a more robust and reliable amplifier solution that can only be facilitated by a combination of high efficiency and good package thermal characteristics.

The exposed pad must be soldered to the PC Board to increase the maximum power dissipation capability of the TAA2009 package. Soldering will minimize the likelihood of an over-temperature fault occurring during continuous heavy load conditions. There should be vias for connecting the exposed pad to the copper area on the printed circuit board.

Conducting initial testing or characterization ***without*** the exposed pad soldered to the printed circuit board will give erroneous case temperature measurements. The TAA2009 is an extremely robust device; so not soldering the device to the printed circuit board, due to potential rework issues, should not be a concern. These devices do not fail unless the operating supply voltages maximums are exceeded, and/or an improper printed board design is utilized.

The maximum device power dissipation, for a given ambient temperature, can be calculated based on a 150°C maximum junction temperature, T_{JMAX}, as given by the following equation:

$$P_{DISS} = \frac{(T_{JMAX} - T_A)}{\theta_{JA}}$$

where:

P_{DISS} = maximum power dissipation
T_{JMAX} = maximum junction temperature of TAA2009
T_A = operating ambient temperature
θ_{JA} = junction-to-ambient thermal resistance = 21°C/W when soldered to PCB

From the above formula, the maximum power dissipation at an ambient temperature of 25°C is 5.95W, and at 85°C is 3.10W.

Performance Measurements of the TAA2009

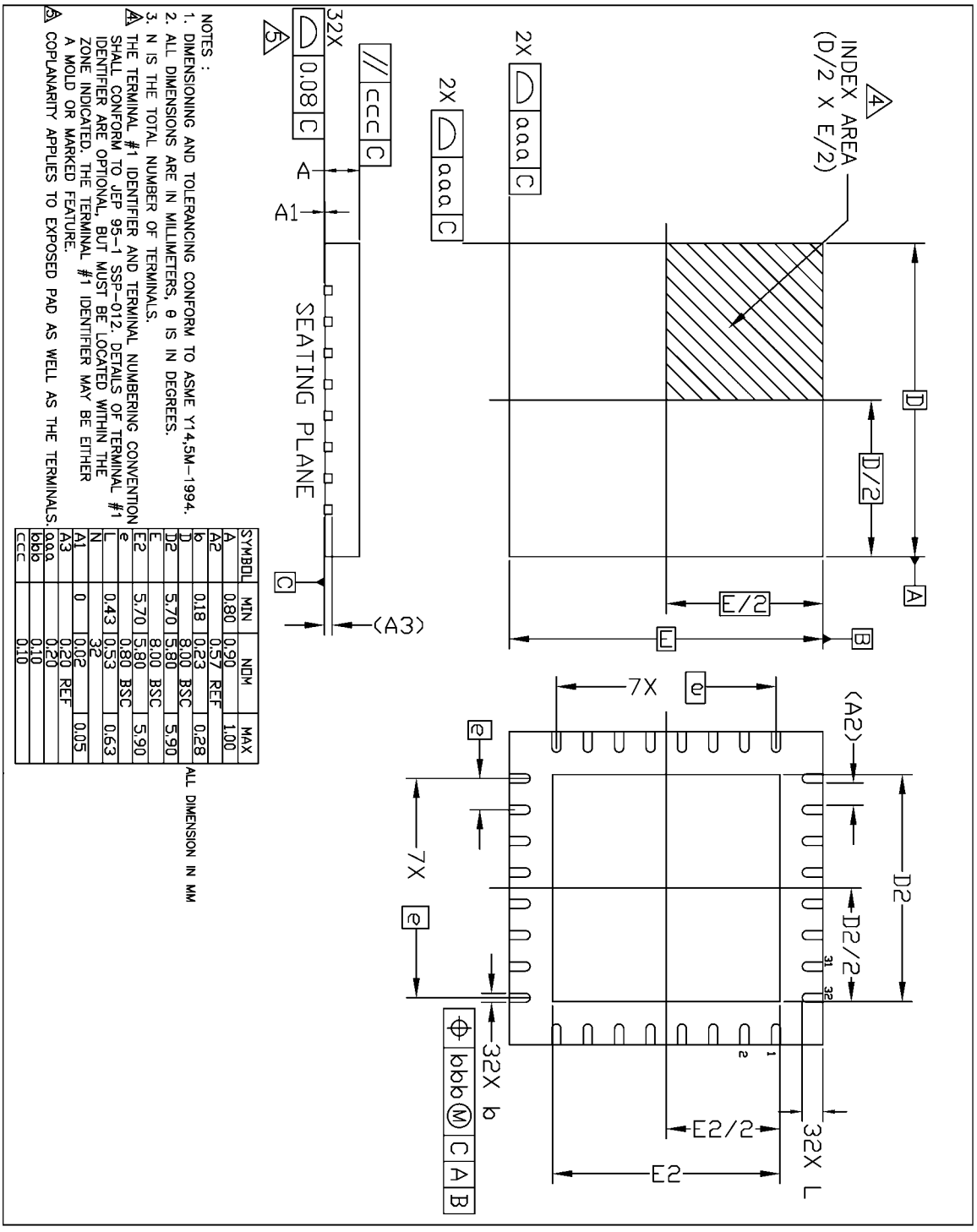
The TAA2009 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 100kHz and 1.0MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the Tripath amplifiers switching pattern will degrade the measurement.

One feature of the TAA2009 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TAA2009 Evaluation Board uses the Test/Application Circuit in this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

PACKAGE INFORMATION

32 PIN QFN - 8MM x 8MM X 1MM



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP 95-1 SSP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. COPLANARITY APPLIES TO EXPOSED PAD AS WELL AS THE TERMINALS.

SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0	0.02	0.05
A3		0.20 REF	
aaa		0.10	
bbb		0.10	
ccc		0.10	

ALL DIMENSION IN MM

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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